WHAT IS CLAIMED IS:

1. An address translation unit performing address translation from a virtual address to a physical address, comprising:

a data entry part holding data of said physical address; and

a tag entry part storing an address space identifier and virtual address as a tag of said data entry part,

said tag entry part comprising:

an address space identifier hold part holding said address space identifier;

an address space identifier comparison judgment part comparing an address space identifier hold value held in said address space identifier hold part with an address space identifier input value to be inputted newly;

a virtual address hold part holding said virtual address; and

a virtual address comparison judgment part comparing a virtual address hold value held in said virtual address hold part with a virtual address input value to be inputted newly,

said virtual address comparison judgment part having a charge circuit for charging its output line and a charge inhibit circuit for inhibiting charge to said output line, wherein a potential state of said output line is controlled based on the comparison result between said address space identifier hold value and said address space identifier input value, to determine execution or non-execution of comparison operation between said virtual address hold value and said virtual address input value at the time of address translation.

2. The address translation unit according to claim 1 wherein

said address space identifier hold part and said virtual address hold part are each configured by a content addressable memory,

a content addressable memory cell configuring said address space identifier hold part is connected to an address space identifier comparison match line and also connected to said address space identifier comparison judgment part,

a content addressable memory cell configuring said virtual address hold part is connected to a virtual address comparison match line and also connected to said virtual address comparison judgment part, and

said virtual address comparison judgment part receives a comparison result signal obtained in said address space identifier comparison judgment part and, when said address space identifier hold value matches said address space identifier input value, maintains said virtual address comparison match line in a floating state and performs a comparison at least between said virtual address hold value and said virtual address input value.

3. The address translation unit according to claim 2 further comprising:

a valid bit part holding information as to whether data of said tag entry part is effective, wherein

said valid bit part is configured by a content addressable memory,

said virtual address comparison match line is also connected to a content addressable memory cell configuring said valid bit part, and

said virtual address comparison judgment part also performs a comparison between a valid bit hold value held in said valid bit part and a valid bit input value to be inputted newly.

4. The address translation unit according to claim 2 wherein

said address space identifier comparison judgment part comprises:

an MOS transistor; and

a latch,

said MOS transistor having a first main electrode connected to a power source, a second main electrode connected to said address space identifier comparison match line, and a control electrode to which a comparison control signal for controlling comparison operation is provided, and

said latch having a data input terminal connected to said address space identifier comparison match line, a control input terminal to which said comparison control signal is provided, and an output terminal outputting said comparison result signal.

5. The address translation unit according to claim 2 wherein

said virtual address comparison judgment part comprises:

first and second MOS transistors that are connected in series and have different conductivity types;

an inverter; and

an OR gate,

said first MOS transistor having a first main electrode connected to a first power source and a second main electrode connected to said virtual address comparison match line,

said second MOS transistor having a first main electrode connected to said virtual address comparison match line and a second main electrode connected to a second power source,

said inverter having an input to which said comparison result signal is provided, and an output connected to a control electrode of said second MOS transistor and one input of said OR gate, and

said OR gate having another input to which a comparison control signal for controlling comparison operation is provided and an output connected to a control electrode of said first MOS transistor.

6. The address translation unit according to claim 2 wherein

said address space identifier comparison judgment part further has a function by which an external signal provided from the exterior is received and one of said comparison result signal and said external signal is selected and provided to said virtual address comparison judgment part, and

said address translation unit further has an output path through which said comparison result signal is outputted to the exterior.

7. The address translation unit according to claim 6 wherein

said address space identifier comparison judgment part comprises:

an MOS transistor;

a latch;

a selector; and

an OR gate,

said MOS transistor having a first main electrode connected to a power source, a second main electrode connected to said address space identifier comparison match line, and a control electrode to which a comparison control signal controlling comparison operation is provided,

said selector to which a selective control signal is provided as a control signal for selective operation and a signal of said address space identifier comparison match line and said external signal are provided as an input signal, said selector providing its output to a data input terminal of said latch,

said OR gate having one input to which said comparison control signal is provided and another input to which said selective control signal is provided, said OR providing its output to a control input terminal of said latch, and

an output terminal of said latch outputting said comparison result signal or said external signal.

8. An address translation unit performing address translation from a virtual address to a physical address, comprising:

a data entry part holding data of said physical address; and

a tag entry part storing an address space identifier and virtual address as a tag of said data entry part,

said tag entry part comprising:

a valid bit part holding information as to whether data of said tag entry part is valid;

an address space identifier hold part holding said address space identifier;

an address space identifier comparison judgment part comparing an address space identifier hold value held in said address space identifier hold part and a valid bit hold value held in said valid bit part, with an address space identifier input value and valid bit input value that are inputted newly;

a virtual address hold part holding said virtual address; and

a virtual address comparison judgment part comparing a virtual address hold

value held in said virtual address hold part with a virtual address input value to be inputted newly, wherein

said virtual address comparison judgment part determining execution or non-execution of comparison operation between said virtual address hold value and said virtual address input value at the time of address translation, based on the comparison result between said address space identifier hold value and said address space identifier input value, and said information as to whether data of said tag entry part is valid or invalid.

9. The address translation unit according to claim 8 wherein

said address space identifier comparison judgment part determines execution or non-execution of comparison operation between said address space identifier hold value and said address space identifier input value, based on said valid bit hold value.

10. The address translation unit according to claim 9 wherein

said address space identifier hold part, said virtual address hold part, and said valid bit part are each configured by a content addressable memory,

a content addressable memory cell configuring said address space identifier hold part and a content addressable memory cell configuring said valid bit part are connected in parallel to each other and also connected to said address space identifier comparison judgment part by an address space identifier comparison match line,

a content addressable memory cell configuring said virtual address hold part is connected to a virtual address comparison match line and also connected to said virtual address comparison judgment part, and

said virtual address comparison judgment part receives a comparison result

signal obtained in said address space identifier comparison judgment part, in which when said address space identifier hold value and said valid bit hold value match said address space identifier input value and said valid bit input value, respectively, said virtual address comparison match line is maintained in a floating state and said virtual address hold value is compared with said virtual address input value.

11. The address translation unit according to claim 10 wherein

said address space identifier comparison judgment part comprises:

an MOS transistor; and

a latch,

said MOS transistor having a first main electrode connected to a power source, a second main electrode connected to said address space identifier comparison match line, and a control electrode to which a comparison control signal for controlling comparison operation is provided, and

said latch having a data input terminal connected to said address space identifier comparison match line, a control input terminal to which said comparison control signal is provided, and an output terminal outputting said comparison result signal.

12. The address translation unit according to claim 10 wherein

said virtual address comparison judgment part comprises:

first and second MOS transistors that are connected in series and have different conductivity types;

an inverter; and

an OR gate,

said first MOS transistor having a first main electrode connected to a first power source and a second main electrode connected to said virtual address comparison match line,

said second MOS transistor having a first main electrode connected to said virtual address comparison match line and a second main electrode connected to a second power source,

said inverter having an input to which said comparison result signal is provided and an output connected to a control electrode of said second MOS transistor and one input of said OR gate, and

said OR gate having another input to which a comparison control signal for controlling comparison operation is provided and an output connected to a control electrode of said first MOS transistor.

13. The address translation unit according to claim 10 wherein

said address space identifier comparison judgment part further has a function by which an external signal provided from the exterior is received and one of said comparison result signal and said external signal is selected and provided to said virtual address comparison judgment part, and

said address translation unit further has an output path through which said comparison result signal is outputted to the exterior.

14. The address translation unit according to claim 13 wherein

said address space identifier comparison judgment part comprises:

an MOS transistor;

a latch;

a selector; and

an OR gate,

said MOS transistor having a first main electrode connected to a power source, a second main electrode connected to said address space identifier comparison match line, and a control electrode to which a comparison control signal for controlling comparison operation is provided,

said selector to which a selective control signal is provided as a control signal of selective operation and a signal of said address space identifier comparison match line and said external signal are provided as an input signal, said selector providing its output to a data input terminal of said latch,

said OR gate having one input to which said comparison control signal is provided and another input to which said selective control signal is provided, said OR gate providing its output to a control input terminal of said latch, and

an output terminal of said latch outputting said comparison result signal or said external signal.

15. The address translation unit according to claim 3 wherein

said virtual address comparison judgment part determines execution or non-execution of comparison operation between said virtual address hold value and said virtual address input value, based on the comparison result between said address space identifier hold value and said address space identifier input value, and said valid bit hold value.

16. The address translation unit according to claim 1 wherein

said virtual address comparison judgment part compares said virtual address

hold value with said virtual address input value at the time of address translation, when said address space identifier hold value matches said address space identifier input value, and does not compare said virtual address hold value with said virtual address input value at the time of address translation, when said address space identifier hold value mismatches said address space identifier input value.

17. The address translation unit according to claim 8 wherein

said virtual address comparison judgment part compares said virtual address hold value with said virtual address input value at the time of address translation, when said address space identifier hold value matches said address space identifier input value and also said valid bit hold value matches said valid bit input value, and does not compare said virtual address hold value with said virtual address input value at the time of address translation, when said address space identifier hold value mismatches said address space identifier input value or said valid bit hold value mismatches said valid bit input value.